



**Model 560-5187-1T
CPU I/O / Timing Input Module Manual**

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SECTION ONE

1. FUNCTIONAL DESCRIPTION

1.1. PURPOSE OF EQUIPMENT

The TrueTime Model 560-5187-1T CPU I/O / Timing Input Module provides an input/output interface, via a Male DB-9 connector (labeled CPU I/O), between the Fault Monitor / CPU and the user. Additionally it provides an input interface to the CPU, via BNC connectors labeled (P and S), for Primary and Secondary Source status. The use of these signals is described in the manual section for the compatible CPU.

In addition to the CPU interface, this card provides inputs, via BNC connectors, that directly drive Timing Signals 7 through 8 on the backplane. INPUT 7 through INPUT 8 on the Module drive signal IN7 and IN8, respectively. The two backplane signals are distributed via controlled-impedance traces, terminated on the backplane at Slot 17. For proper operation, the 50 ohm terminator for each Timing Signal **must** be enabled or disabled to match the driving source (see the Chassis Manual for information).

1.1.1. PHYSICAL SPECIFICATIONS

Dimensions: 0.8" w X 4.4" h X 5.0" d (2 cm X 11 cm X 13 cm)
Weight: Approximately ½ pound (¼ kg)

1.1.2. ENVIRONMENTAL SPECIFICATIONS

Operating Temp: 0° to +50°C
Storage Temp: -40° to +85°C
Humidity: 95% relative, non-condensing
Cooling Mode: Convection

1.1.3. POWER REQUIREMENTS

Power: None

1.1.4. CPU INPUT/OUTPUT

Connector Type: DB-9M

Connector Pinout:

Pin 1:	OUT 1	
Pin 2:	RXD / RS-232 In	Pin 6: RIN- / Differential- In
Pin 3:	TXD / RS-232 Out	Pin 7: RIN+ / Differential+ In
Pin 4:	OUT 2	Pin 8: TOUT- / Differential- Out
Pin 5:	SIGNAL GND	Pin 9: TOUT+ / Differential+ Out

1.1.5. STATUS INPUTS S AND P

Connector Type: BNC
Signal Type: As specified in manual for compatible CPU.

1.1.6. INPUTS 7 AND 8

Connector Type: BNC
Input Impedance: Selectable: 50 ohm / High (see Chassis Manual)
Signal Type: As specified for card(s) using input signal.

1.1.7. CARD COMPATIBILITY

Location: Slots 1-3, with compatible card in front slot.
Compatibility: See Card Compatibility Matrix.

SECTION TWO

2. INSTALLATION AND OPERATION

2.1. HOT-SWAPPING

All cards, input cables and output cables are hot swappable. It is not necessary to remove chassis power during insertion or removal. The system is designed to protect against permanent effects and minimize any temporary effects of hot swapping.

2.2. REMOVAL AND INSTALLATION

Refer to CARD COMPATIBILITY section prior to installing new card.

To remove card, loosen the captive retaining hardware at the top and bottom of the assembly, then firmly pull on the handle (or on any connector on rear panel adapter cards) at the bottom of the card. Slide the card free of the frame. Refer to the SETUP section for any required switch settings; or, set them identically to the card being replaced. Reinstall the card in the frame by fitting it into the card guides at the top and bottom of the frame and sliding it in slowly, avoiding contact between bottom side of card and adjacent card front panel, until it mates with the connector. Seat card firmly to avoid contact bounce. Secure the retaining screws at the top and bottom of the card assembly.

2.3. SETUP

This card has no setup requirements. However, for proper operation, the 50 ohm terminator for each Timing Signal **must** be enabled or disabled to match the driving source (see the Chassis Manual for information).

2.4. FAULT INDICATION

This card has no fault indication.

2.5. MAINTENANCE

This card has no maintenance requirements.

SECTION THREE

3. THEORY OF OPERATION

3.1. GENERAL INFORMATION

This section contains a detailed description of the circuits in the CPU I/O Module. These descriptions should be used in conjunction with the drawings in SECTION FOUR.

3.2. HARDWARE DESCRIPTION

The Module incorporates various connectors and comes in various configurations controlled by component installation. Use the Bill of Materials in conjunction with the Schematic to determine the exact configuration of this version.

The DB-9M connector, J5, supports RS-232 and differential communications to/from the CPU and a status output from the CPU. The signaling protocol is dependent on the card installed in the front slot.

The Module also has two BNC connectors, J1 and J2, which are used as status inputs as defined in the compatible CPU manual.

The two Timing Signal inputs are supported via BNC connectors J3 (INPUT 7) and J4 (INPUT 8), which drive backplane signals IN7 and IN8 respectively. These signals are distributed via 50 ohm traces and DC-coupled to the backplane. On the backplane, they are terminated at Slot 17 with switch-enabled 50 ohm termination resistors. As a result of this architecture, this card must be located at or near Slot 1 with all Timing Signal users located in higher slots. Each termination resistor **must** be enabled or disabled to match the signal source.

SECTION FOUR

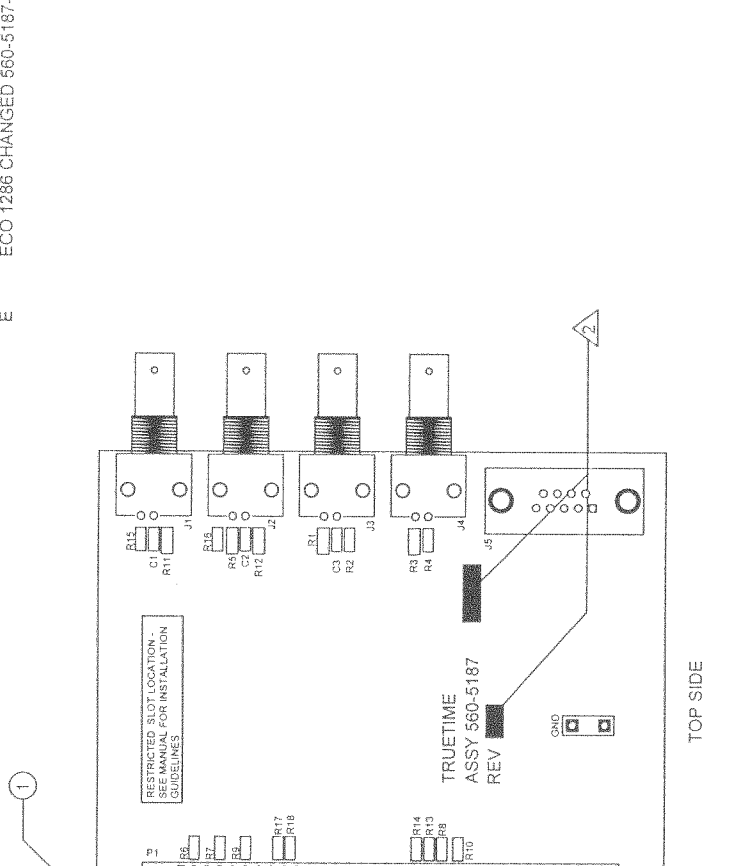
4. DETAILED DRAWINGS

4.1. 560-5187-1T DETAILED DRAWINGS / BILL OF MATERIALS

MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
560-5187-1T	CPU I/O MODULE, QUAD INPUT MADE FROM 560-2187						EA	
0000-APPROVAL	PARTS LIST APPROVAL		000000		1.0000		EA	<i>1/99</i>
0000-PL	PARTS LIST REV LEVEL		000000		1.0000		EA	REV E (01-29-99)
0000-PRINT	REFERENCE PRINT		000000		1.0000		EA	SEE 560-5187
0000-REV	PCB REV LEVEL HERE >>>>		000000		1.0000		EA	560-2187 REV C
002S-000	RES 0 OHM 1/4W 0805	NIC NRC10Z0TR	000000		6.0000		EA	R2,4,8,10,17,18
002S-787R	RES 78.7 OHM 1/4W 1206 1%	NIC NRC12F78R7TR	000000		2.0000		EA	R11,12
223-138	SCREW SH CH ZN M2.5X10	SCHROFF #21100-138	000000		2.0000		EA	03
223-144	NUT M2.5	SCHROFF #21100-144	000000		2.0000		EA	04
223-379	SCREW CAP NP M2.5 X 11	SCHROFF #21100-379	000000		2.0000		EA	07
223-464	SLEEVE, STAINLESS	SCHROFF 21100-660	000000		2.0000		EA	08
273-009	TERMINAL TEST POINT	COMP CORP PJ-201-25	000000		1.0000		EA	GND
372-09P	CONN 9-P D-SUB RT ANG ML	AMP 748879-1 (BOM NAV)	000000		1.0000		EA	J5
372-609-003	JACK SOCKET SET OF 2	THOMAS & BETTS 609-003	000000		1.0000		EA	FOR J5
372-96RA	CONN, 96-P FM DIN RT ANGLE	BERG 68353-296	000000		1.0000		EA	P1
375-022	LOCKWASHER, BNC PC MT	AMP 1-329632-2	000000		4.0000		EA	10
375-023	NUT BNC PC MT	AMP 1-329631-2	000000		4.0000		EA	
	05 (J1-J4) DO NOT USE THE NUT THAT COMES WITH THE CONNECTOR.							
375-227677-1	CONN BNC PC MT	AMP 227677-1	000000		4.0000		EA	06 (J1-J4)
391-004	ADAPTER FOR RS PORT	FAITECH MCM70029	000000		1.0000		EA	SHIPPING KIT
560-1231-2	REAR PNL, CPU I/O QUAD	SCREEN	000000		1.0000		EA	02
560-2187	CPU I/O MODULE, QUAD INPUT FAB		000000		1.0000		EA	01
LA	LABOR ASSEMBLY COST HRS		000000		0		EA	
LT	LABOR TEST COST HOURS		000000		0		EA	
NOTE 1			000000		1.0000		EA	
	DO NOT INSTALL: R1,R3,R5,R6,R7,R9,13-16 C1,C2,C3							
OSV560-5187-1T	OUTSIDE LABOR 560-5187-1T PCA		000000		1.0000		EA	

NOTES: UNLESS OTHERWISE SPECIFIED
 1. RESISTORS ARE IN OHMS AND CAPACITORS ARE IN MICRO FARADS
 2. STAMP REVISION LEVEL AND DASH NUMBER
 3. ASSEMBLE PER ASSEMBLY REQUIREMENTS
 DOCUMENT 421-11.



TOP SIDE

REVISIONS		
LTR	DESCRIPTION	DATE
A	J5 MOVED BACK .100"	8-1-97
B	DESIGN UPDATE	9-19-97
C	ECO 1153 MOVE TRACE (CAR #731)	4-30-98
D	CAR 1381	1-25-99
E	ECO 1286 CHANGED 560-5187-2F VIEW	12-16-99

TrueTime, Inc.
 Santa Rosa, California

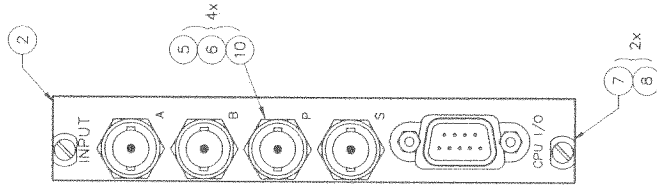
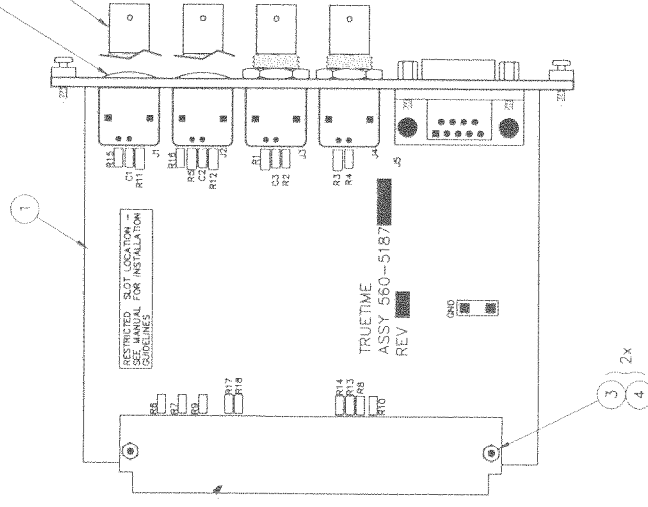
Title		ASSY DRAWING	
CPU I/O QUAD INPUT MODULE		Rev	
Size	B	Number	560-5187
Date	12-16-99	File Name	2187C.PCB
S.B.K.		S.B.K.	
Sheet 1		of 3	

CONTRACT NO.	APPROVALS	DATE
	S.B.K.	5-4-97
DRAWN BY	CHECKED	APPROVED
S.B.K.		
NEXT ASSY		

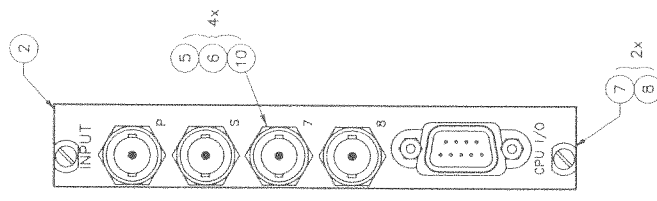
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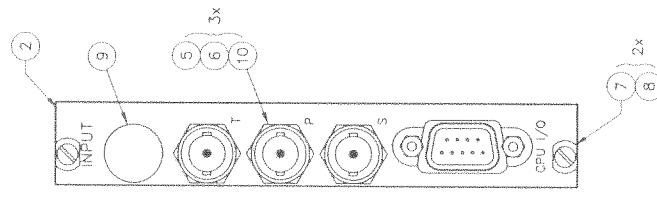
FOR -1F & -1T ASSEMBLIES ONLY



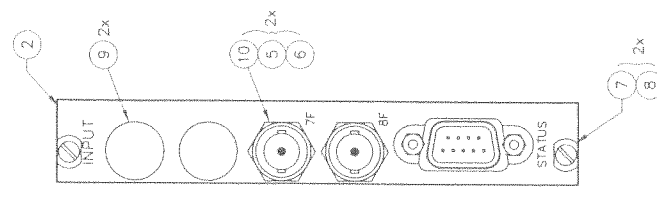
-1F
REFERENCE MODE
VERSION



-1T
STATUS & TIMING
VERSION



-1S
STATUS
VERSION



-2F
INPUT MODE
VERSION

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 2835 Duke Ct. Santa Rosa, CA 95407

SIZE	CODE	IDENT NO.	DRAWING NO.	REV
B			560-5187	E

SCALE: NONE SHEET 2 OF 3

FILENAME: \560\5187
 DATE: 12-14-99